RESPONSE

Claims 1-29 were pending in the Application. Claims 1-12 and 14-29 are rejected. Upon entry of the present Response, claims 1-29 are pending and presented for reconsideration.

The present Amendment amends paragraph [0034] of the specification to correct a single digit in the Serial Number of the cited co-pending application. Applicant submits that no new matter has been introduced.

Allowable Subject Matter

Applicant thanks the Examiner for acknowledging that claim 13 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Rejection of Claims Under 35 U.S.C. §102

Claims 1-4 and 6-12 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,815,647 to Buckland et al. (hereinafter "Buckland"). Claims 1-2, 4-5, 7-10, and 14-29 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,032,271 to Goodrum et al. (hereinafter "Goodrum"). The Applicant respectfully traverses the rejections.

Buckland

Buckland "relates to computer systems having a central processing unit (CPU) and plural devices, or feature cards for performing specific system functions." Col. 1, lines 23-26. Buckland addresses the need "for a system that would allow a CPU to identify which specific device on a particular adapter card generated an error signal." Col. 1, lines 62-64. Buckland further discloses error recovery techniques. Abstract.

Specifically, Buckland teaches "a computer system having additional control logic . . . provided with a bridge chip and at least one connector slot for receiving a feature card, that implements specific functions such as I/O, memory, or the like." Col. 2, lines 23-26. "This chip

provides the interface between the I/O bus and the actual adapter slot 106 which includes a connector 4 and additional logic." Col. 6, lines 12-15.

Buckland includes a schematic diagram illustrating the signals required for I/O adapter slots to be isolated. Col. 2, line 66, through col. 3, line 2, and Figure 9. Buckland also includes a flow chart that includes isolation in the error recovery. Col. 3, lines 3-4, and Figure 10. As Buckland's Figure 9 shows, "[t]he I/O bus 102 . . . is connected to a bridge chip 104, and in combination with the additional control logic 105, is used to control a single PCI slot 106." Col. 6, lines 48-50. "One modified bridge chip 104 in conjunction with one set of control logic 105 is used to control one slot 106." Col. 6, lines 56-58.

Buckland isolates a device in response to an error signal associated with the device. Figure 10. As Buckland explains with respect to Figure 10:

> [If a system error signal] SERR# signal is present from one of the plurality of devices on the adapter cards in the computer system . . . , the reset signal RST# is activated (by bridge chip 104) to the device signaling SERR#, to place the device 5 in its reset state and avoid any damage to the system, while still keeping the device coupled to the system. That is, the slot 106 having the feature card which issued the SERR# signal is reset in the manner previously described (data processing activity is ceased). At step 5, the status bit in register 203 is set, e.g. to logical 1. Next, at step 6, the control hardware as shown in FIG. 9 will ignore all load and store operation, and abort any pending direct memory access (DMA) operations. . . . If there are no additional load/store operations, then at step 8 the device driver reads the status bit in register 203 of bridge chip 104. . . . However, if at step 5 the status bit was set to indicate the presence of an SERR# signal, then bridge chip 104 is reconfigured (by re-initialization) at step 11. Typically the device driver will reset the feature card by re-initializing the device. . . . Thus, it can be seen how the present invention allows a computer system to isolate a single device in a particular I/O slot 106 . . . .

Col. 12, line 61, through col. 13, line 42 (emphasis added). In summary, Buckland isolates a device in response to a single signal, namely, an SERR# signal.

Comparison of Claim 1 to Teachings of Buckland

The Office Action suggests Buckland discloses an apparatus that includes all of the elements of independent claim 1. Pages 2-3.

Claim 1 is an apparatus for isolating a device from a bus without interrupting system operation that recites, in part: "wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal and a received device isolation signal." As the foregoing element of claim 1 indicates, an isolation switch control signal is transmitted in response to two signals—"the generated bus status signal" and "a received device isolation signal."

As explained above, Buckland teaches an apparatus that isolates a device in response to one signal. Buckland does not teach an apparatus "wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal and a received device isolation signal" as recited in claim 1. Therefore, Applicant respectfully submits that Buckland does not teach or suggest all of the limitations of claim 1.

Claims 2-4 and 6-12 depend from claim 1 and include all of the limitations of claim 1. Since, as explained above, Buckland does not teach or suggest all of the elements of claim 1, Buckland cannot teach or disclose all of the elements of the claims that depend from that claim.

Therefore, in light of the foregoing reasons, Applicant respectfully requests that the rejection of claims 1-4 and 6-12 as being anticipated by Buckland under 35 U.S.C. §102 be reconsidered and withdrawn.

Goodrum

Goodrum "relates to fault isolation." Col. 1, line 7. Generally, Goodrum "features a computer system having devices, mass storage accessible by at least one of the devices, and a watcher for monitoring for a faulty condition." Col. 1, lines 21-24. Goodrum teaches that "[t]he devices are coupled to a bus, and the faulty condition includes a bus hang condition." Col. 1, lines 38-40. "The watcher includes a bus timer to monitor the bus to detect the bus hang condition." Col. 1, lines 40-41. "The bus hang condition is present if the bus timer expires."

Col. 1, lines 41-42. Further, Goodrum teaches that a "fault isolation controller is used to turn off the devices when the bus hang condition is detected and to turn the devices back on to test the devices." Col. 1, lines 42-45. "The faulty device is identified if the bus hang condition occurs when that device is tested." Col. 1, lines 46-48.

Specifically regarding fault isolation, Goodrum explains:

> The bus watcher 129 can detect for a hang condition on the secondary PCI bus 32. If a hang condition is detected, the bus watcher 129 sets a bus hang pending bit, which causes the SIO 50 to power down to slots on the secondary PCI bus 32 and a non-maskable interrupt (NMI) to be transmitted to the CPU 14. The CPU 14 responds to the NMI by invoking an NMI routine to isolate the slot(s) causing the hang condition. Once identified, the defective slot(s) are disabled or powered off.

Col. 86, lines 56-64. Goodrum describes the second part of the process in more detail with respect to Figure 37:

> Referring to FIG. 37, the NMI handler first determines 400 if the bus hang pending bit is set by reading the bus hang indication register 482. If so, the NMI handler calls 401 a BIOS isolation handler for isolating the defective slot or slots. Otherwise, other NMI procedures are called 402.

Col. 87, lines 59-64. In Goodrum, a device is isolated in response to the detection of a bus hang condition. Figure 37.

In Goodrum, the watcher includes a bus timer to monitor only one thing, the "bus hang condition;" detection of the "bus hang condition" causes the fault isolation controller to turn off the devices causing the "bus hang condition." Col. 1, lines 40-44. In summary, Goodrum isolates a device solely in response to the detection of one signal, namely a "bus hang condition".

Comparison of Claim 1 to Teachings of Goodrum

The Office Action suggests Goodrum discloses an apparatus that includes all of the elements of independent claim 1. Pages 6-7.

Claim 1 recites, in part: "wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal and a received device isolation signal." As the foregoing element of claim 1 indicates, an isolation switch control signal is transmitted in response to two signals —"the generated bus status signal and a received device isolation signal."

As explained above, Goodrum teaches an apparatus that isolates a device in response to only one signal, a bus hang condition. Goodrum does not teach an apparatus "wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal and a received device isolation signal" as recited in claim 1. Therefore, Applicant respectfully submits that Goodrum does not teach or suggest all of the limitations of claim 1.

Claims 2, 4, 5, 7-10, and 14-18 depend from claim 1 and include all the limitations of claim 1. Since, as explained above, Goodrum does not teach or suggest all of the elements of claim 1, Goodrum cannot teach or disclose all of the elements of the claims that depend from that claim.

Therefore, in light of the foregoing reasons, Applicant respectfully requests that the rejection of claims 1, 2, 4, 5, 7-10, and 14-18 as being anticipated by Goodrum under 35 U.S.C. §102 be reconsidered and withdrawn.

Comparison of Claims 19 and 24 to Teachings of Goodrum

The Office Action further suggests Goodrum discloses a computer system that includes all of the elements of independent claims 19 and 24. Pages 9-10.

Claim 19 is a method for isolating the bus device from the bus that, among other steps, includes the step of: "transmitting an isolation switch control signal responsive to both the received device isolation signal and the received bus status signal." Similarly, claim 24 is an apparatus for isolating a device from a bus that includes, in part: "means for transmitting an isolation switch control signal responsive to both the received bus device isolation signal and the received bus status signal." The foregoing claims are similar in that claim 19 includes the step of

transmitting a signal responsive to two other signals whereas claim 24 includes a means for transmitting a signal responsive to two other signals.

As explained above, Goodrum turns devices off based only on the monitoring of a single bus hang condition. Goodrum does not teach a method for isolating the bus device from the bus that includes "transmitting an isolation switch control signal responsive to both the received device isolation signal and the received bus status signal" as recited in claim 19. Likewise, Goodrum does not teach "means for transmitting an isolation switch control signal responsive to both the received bus device isolation signal and the received bus status signal" as recited in claim 24.

Claims 20-23 depend from claim 19 and include all the limitations of claim 19. Claims 25-29 depend from claim 24 and include all the limitations of claim 24. Since, as explained above, Goodrum does not teach or suggest all of the elements of claim 19 or claim 24, Goodrum cannot teach or disclose all of the elements of the claims that depend from those claims.

Therefore, in light of the foregoing reasons, Applicant respectfully requests that the rejection of claims 19-29 as being anticipated by Goodrum under 35 U.S.C. §102 be reconsidered and withdrawn.

SUMMARY

Claims 1-29 are pending in the Application. No claims were amended. Applicant requests that the Examiner reconsider the application and claims in light of the foregoing Response, and respectfully submits that the claims are in condition for allowance. If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Applicant believes that no fees are necessitated by the present Response. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Attorney's Deposit Account No. 20-0531.

Regards,

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